AMENDMENTS TO THE CLAIMS

The listing of claims below replaces all prior versions, and listings, of claims:

- 1 1. (Original) A method, comprising:
- 2 providing a semiconductor substrate;

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- forming electrically conductive columns on the semiconductor substrate;
- forming electrically conductive rows crossing over the electrically conductive columns;
- forming a plurality of memory components each having a resistance value corresponding to multiple logical bits; and
- forming non-volatile memory cells, each formed by connecting a memory component between an electrically conductive row and an electrically conductive column.
- 2. (Original) A method as recited in claim 1, wherein each memory component is formed to have a resistance value based on a thickness of electrically resistive material that forms an individual memory component.
 - 3. (Original) A method as recited in claim 1, wherein each memory component is formed to have a resistance value based on an area of electrically resistive material that forms an individual memory component.
 - 4. (Original) A method as recited in claim 1, wherein each memory component is formed to have a resistance value based on a geometric shape of electrically resistive material that forms an individual memory component.
- 5. (Original) A method as recited in claim 1, wherein the plurality of memory components are each formed to have a different resistance value based on a different area of electrically resistive material that forms a memory component.

1	6. (Original) A method as recited in claim 1, wherein the plurality of
2	memory components are each formed to have a resistance value based on a rectangular
3	geometric shape of electrically resistive material that forms a memory component, at
4	least some of the rectangular geometric shapes having different resistance values
5	corresponding to an area of a rectangular geometric shape.
1	7. (Original) A method as recited in claim 1, wherein forming the
2	non-volatile memory cells comprises:
3	forming a first memory cell having a memory component that indicates logical
4	bits 00 (zero-zero);
5	forming a second memory cell having a memory component that indicates logical
6	bits 01 (zero-one);
7	forming a third memory cell having a memory component that indicates logical
8	bits 10 (one-zero); and
9	forming a fourth memory cell having a memory component that indicates logical
10	bits 11 (one-one).
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1	8. (Original) A method as recited in claim 1, wherein forming the
2	non-volatile memory cells comprises:
3	forming a first memory cell that indicates logical bits 00 (zero-zero)
4	corresponding to a first resistance value based on an area of electrically resistive material
5	that forms a memory component in the first memory cell;
6	forming a second memory cell that indicates logical bits 01 (zero-one)
7	corresponding to a second resistance value based on an area of electrically resistive
8	material that forms a memory component in the second memory cell;
9	forming a third memory cell that indicates logical bits 10 (one-zero)
10	corresponding to a third resistance value based on an area of electrically resistive material
11	that forms a memory component in the third memory cell; and
12	forming a fourth memory cell that indicates logical bits 11 (one-one)
13	corresponding to a fourth resistance value based on an area of electrically resistive
14	material that forms a memory component in the fourth memory cell.

- 9. (Original) A method as recited in claim 1, wherein forming the plurality of memory components comprises forming individual memory components with a resistor in series with a diode.
- 1 10. (Original) A method as recited in claim 1, further comprising configuring
 2 the resistance value of an individual memory component by exposing the memory
 3 component to light.
- 1 11. (Original) A method as recited in claim 1, further comprising configuring
 2 the resistance value of an individual memory component by exposing electrically
 3 resistive material forming the memory component to light.
- 1 12. (Original) A method as recited in claim 1, further comprising configuring 2 the resistance value of an individual memory component by exposing the memory 3 component to heat.
- 1 13. (Original) A method as recited in claim 1, further comprising configuring 2 the resistance value of an individual memory component by exposing electrically 3 resistive material forming the memory component to heat.

1	14. (Original) A method as recited in claim 1, wherein forming the
2	non-volatile memory cells comprises:
3	forming a first non-volatile memory cell by connecting a first memory component
4	between an electrically conductive row and a first electrically conductive column, the
5	first non-volatile memory cell formed as part of a first layer of non-volatile memory cells
6	and
7	forming a second non-volatile memory cell by connecting a second memory
8	component between the electrically conductive row and a second electrically conductive
9	column, the second non-volatile memory cell formed as part of a second layer of
10	non-volatile memory cells.
1	15. (Withdrawn) A method of making a non-volatile read-only memory
2	device, comprising:
3	providing a semiconductor substrate;
4	forming a first layer on the semiconductor substrate;
5	forming one or more additional layers over the first layer;
6	wherein forming an individual layer comprises:
7	forming a plurality of conductive traces; and
8	forming a plurality of memory components each having a resistance value
9	corresponding to multiple logical bits where each memory component is connected
10	between a first conductive trace and a second conductive trace.
1	16. (Withdrawn) A method of making a non-volatile read-only memory
2	device as recited in claim 15, wherein the plurality of memory components are each
3	formed to have a resistance value based on a thickness of electrically resistive material
4	that forms a memory component.
1	17. (Withdrawn) A method of making a non-volatile read-only memory
2	device as recited in claim 15, wherein the plurality of memory components are each
3	formed to have a resistance value based on an area of electrically resistive material that
4	forms a memory component.

1	18. (Withdrawn) A method of making a non-volatile read-only memory
2	device as recited in claim 15, wherein the plurality of memory components each have a
3	resistance value based on a geometric shape of electrically resistive material that forms a
4	memory component, at least some of the geometric shapes having different resistance
5	values corresponding to an area of the geometric shapes.
1	19. (Withdrawn) A method of making a non-volatile read-only memory
2	device as recited in claim 15, wherein forming the plurality of memory components
3	comprises:
4	forming a first memory component having a resistance value corresponding to
5	logical bits 00 (zero-zero);
6	forming a second memory component having a resistance value corresponding to
7	logical bits 01 (zero-one);
8	forming a third memory component having a resistance value corresponding to
9	logical bits 10 (one-zero); and
10	forming a fourth memory component having a resistance value corresponding to
11	logical bits 11 (one-one).
1	20. (Withdrawn) A method of making a non-volatile read-only memory
2	device as recited in claim 15, wherein forming the plurality of memory components
3	comprises forming individual memory components with a resistor in series with a diode.
1	21. (Withdrawn) A method of making a non-volatile read-only memory
2	device as recited in claim 15, further comprising configuring the resistance value of
3	individual memory components by exposing a memory component to light.
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1	22. (Withdrawn) A method of making a non-volatile read-only memory
2	device as recited in claim 15, further comprising configuring the resistance value of
3	individual memory components by exposing a memory component to heat.